

13 and

14 (e) if said timing analysis of said circuit
15 indicates improvement in a worst case delay through said
16 circuit [,],
17

18 (f) then retaining said tapered gate,
and

1 (g) if said timing analysis of said circuit indicates
2 no improvement in said worst case delay through said circuit
3 [,],
4

5 (h) then swapping said tapered gate back to said
6 selected gate for use in said circuit.
7

2. (Currently Amended) The logic synthesis method of claim 1
1 wherein

2 said gate is selected from a gate library comprising a
3 set of non-tapered gates and a set of tapered gates, and
4 wherein in said gate library,
5 said non-tapered gates are characterized by a stack of
6 devices of the same width and said tapered gates are
characterized by a stack of devices of different widths.

1 3. (Currently Amended) The logic synthesis method of claim 1
2 wherein said gate is selected from a gate library
3 comprising a set of non-tapered gates and a set of tapered
gates,
1 and wherein each set in said gate library comprises one or
2 more of the following gates: NAND gates, NOR gates,
3 AND-OR-INVERT gates, and OR-AND-INVERT gates.
4

2 4. (Currently Amended) A logic synthesis method as in claim
3 3 whereby the delay through said tapered gate and the
4 delay through said non-tapered gate are compared.

1 6. (Currently Amended) A logic synthesis method as in claim
2 1 whereby a plurality of tapered gates exist for a
3 non-tapered gate, said plurality of tapered gates being
 functionally equivalent to said non-tapered gate.

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2 7. (Currently Amended) A logic synthesis method as in claim
3 6 whereby the selection of said plurality of tapered gates
 available for use in said circuit is swapped into said
 circuit for comparison with a timing analysis of the
 circuit.

8. (Currently Amended) A logic synthesis method as in claim
7 whereby the delay through said plurality of tapered
 gates and the delay through said non-tapered gate are
 compared.

9. (Currently Amended) A logic synthesis method as in claim
8 whereby the gate of said plurality of gates which yields
 the shortest delay is the one retained for said circuit.